

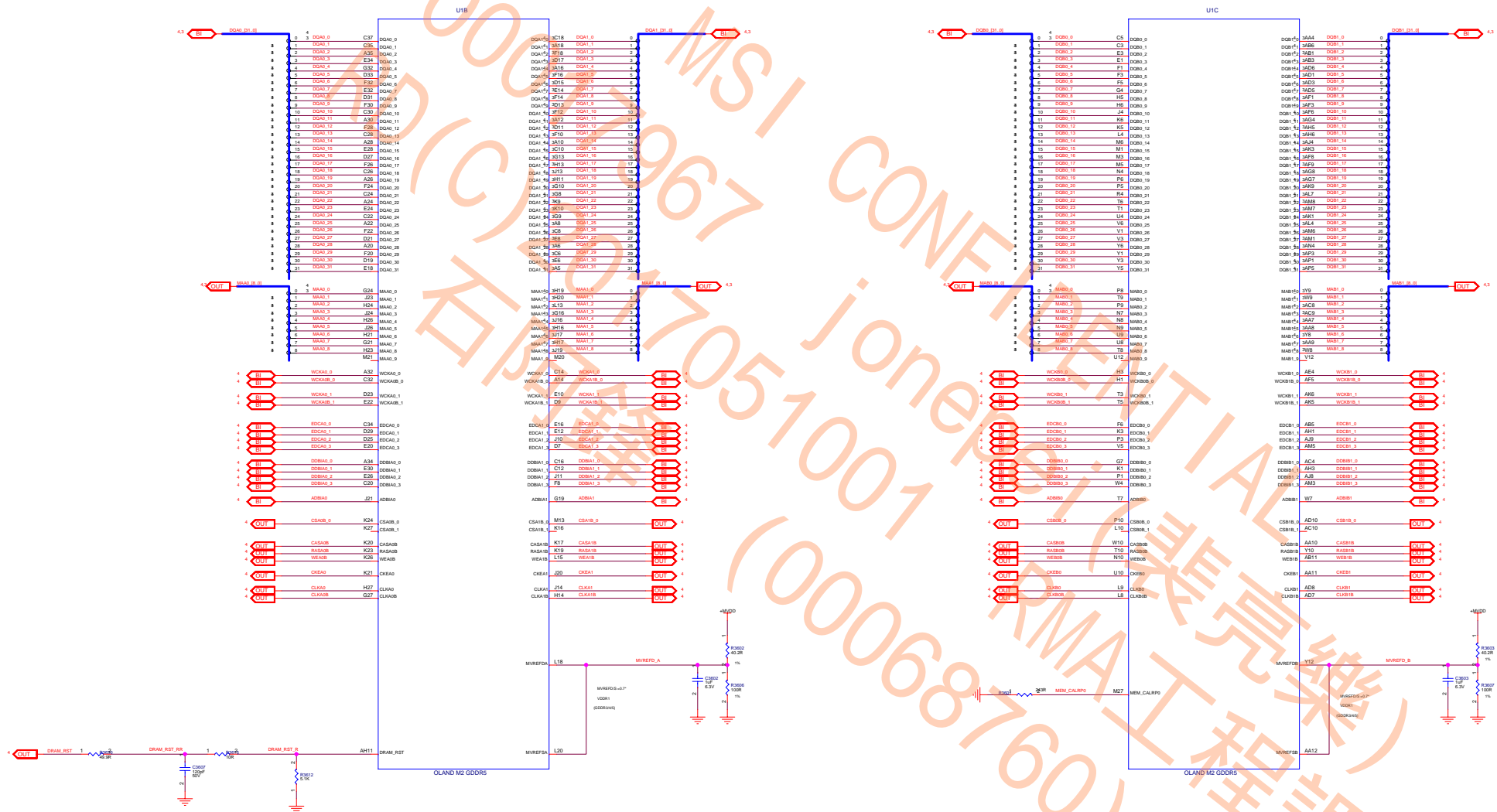
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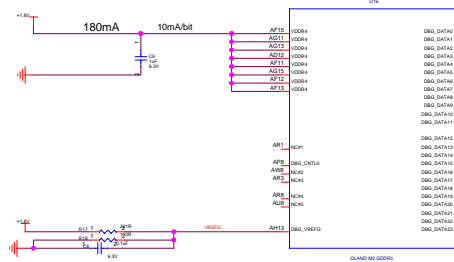
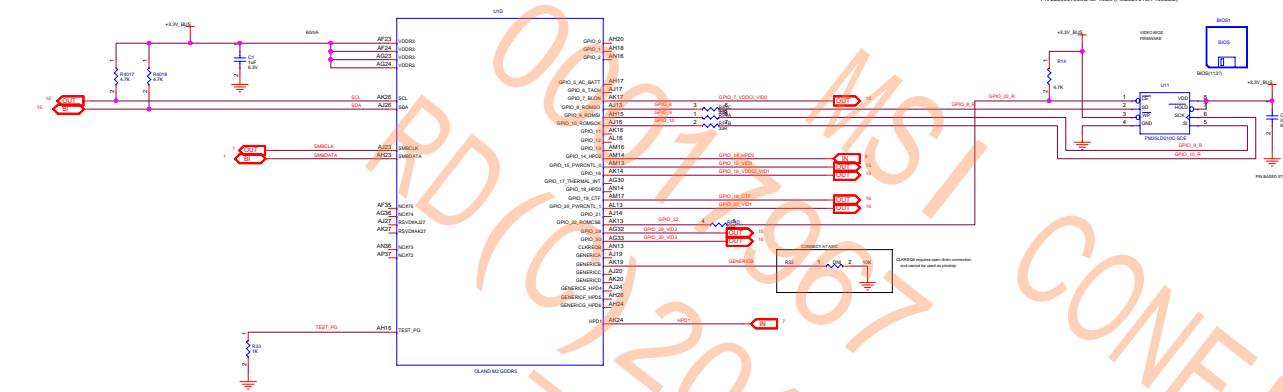
REV: 2.0

TITLE: Oland G5 2GB VGA/sDVI-I+HDMI/DP

DOCUMENT NUMBER: 105-C869xx-00B

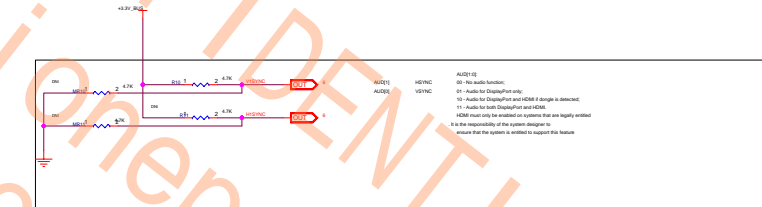
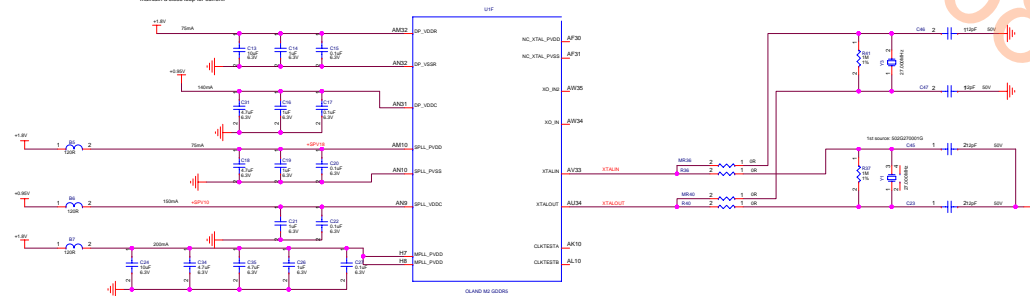


OLAND GPIOs Strap CF XTAL OSC



Place the crossfire
testpoints near the ASIC and
not the connector

Please pay attention to the grounding strategies for these filter capacitors to maintain a close loop for current.



AMD - PLATFORM HARDWARE ENG
#48, No. 1387, ZHANGDONG ROAD
SHANGHAI, CHINA 201203

SHEET: 01 of 02 C:\msd\GPO\STRAP.FLL

DATE: Mon Sep 21 10:05:39 2015

SHEET NUMBER: 5 OF 20

DOCUMENT NUMBER: 105-C862not-008

NOTES:	NOTE
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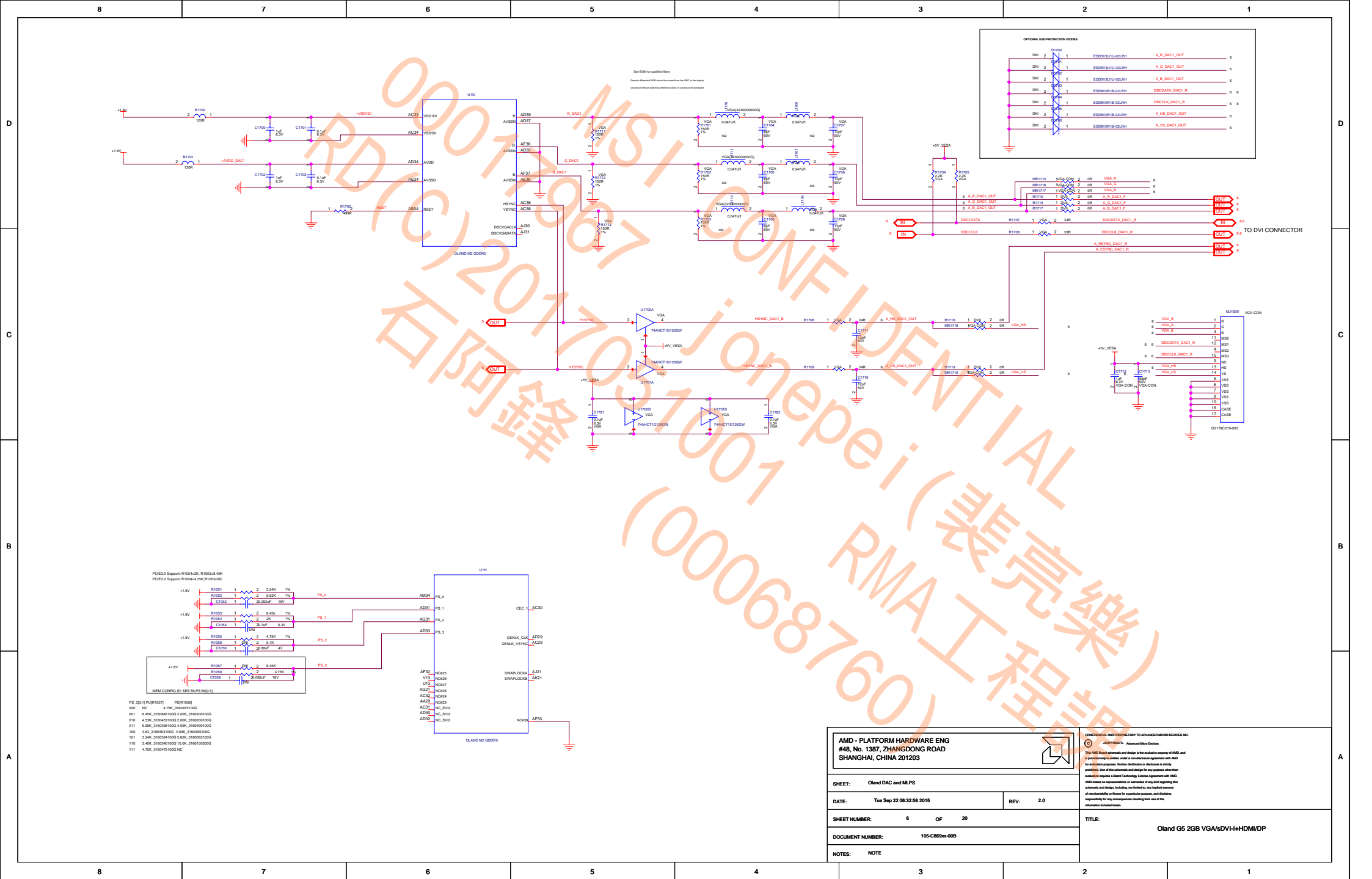
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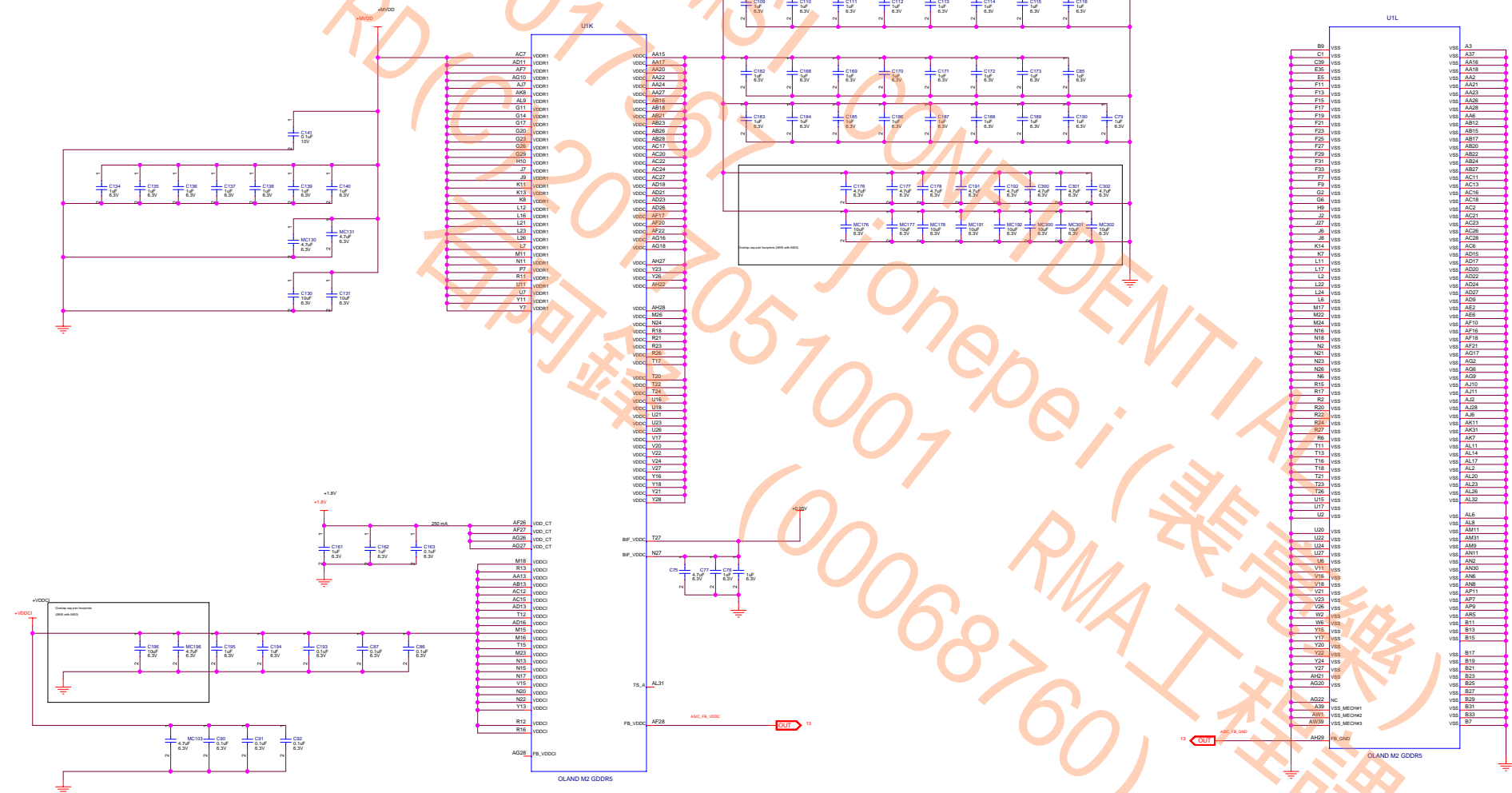
TITLE:	
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Oland G5

Oland G5 2GB VGA/sDVI-I+HDMI/DP



OLAND Power & GND



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SHEET: Oland Power&GND

DATE: Mon Sep 21 10:05:46 2015

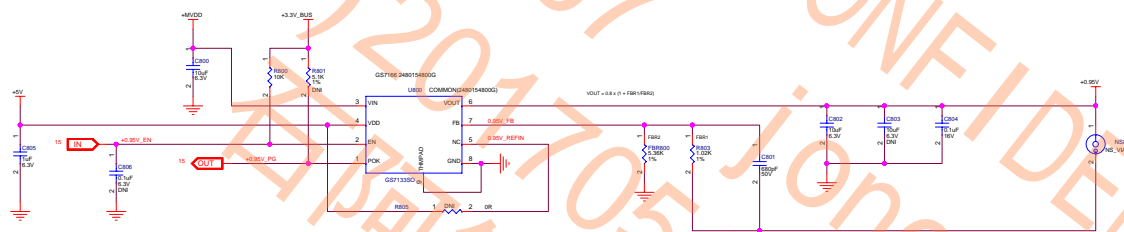
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SHEET NUMBER: 9 OF 20

TITLE: Oland G5 2GB VGA/sDVI-I+HDMI/DP

DOCUMENT NUMBER: 105-C869xx-00B

LDO #1:	$V_{in} = +1.5V \pm 2\%$	$V_{out} = +0.95V \pm 2\%$	$I_{out} = 1.44A$ (TYP) RMS MAX
PCB: 50 to 70mm sq. copper area for cooling			



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SHEET: 0.00V		
DATE: Mon Sep 21 10:05:44 2015		REV: 2.0
SHEET NUMBER: 10 OF 20		
DOCUMENT NUMBER: 105-C869ccr-00B		

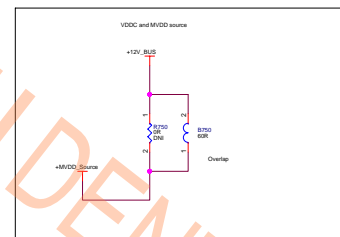
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TITLE:

Oland G5 2GB VGA+SDV+HDMI/DP



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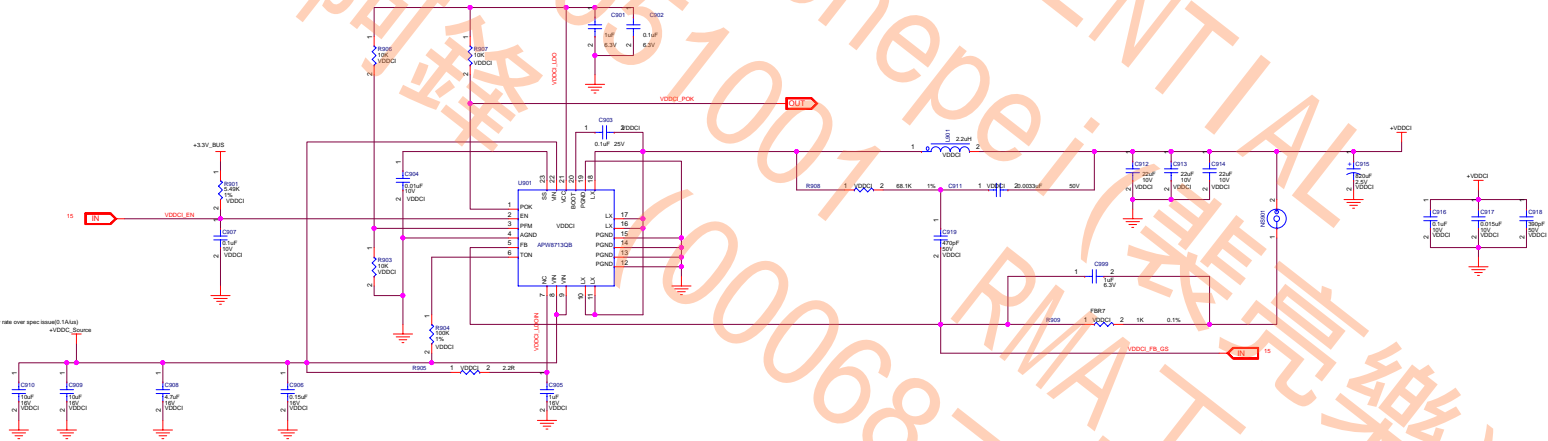
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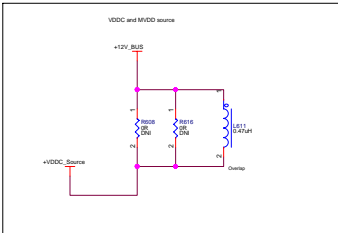
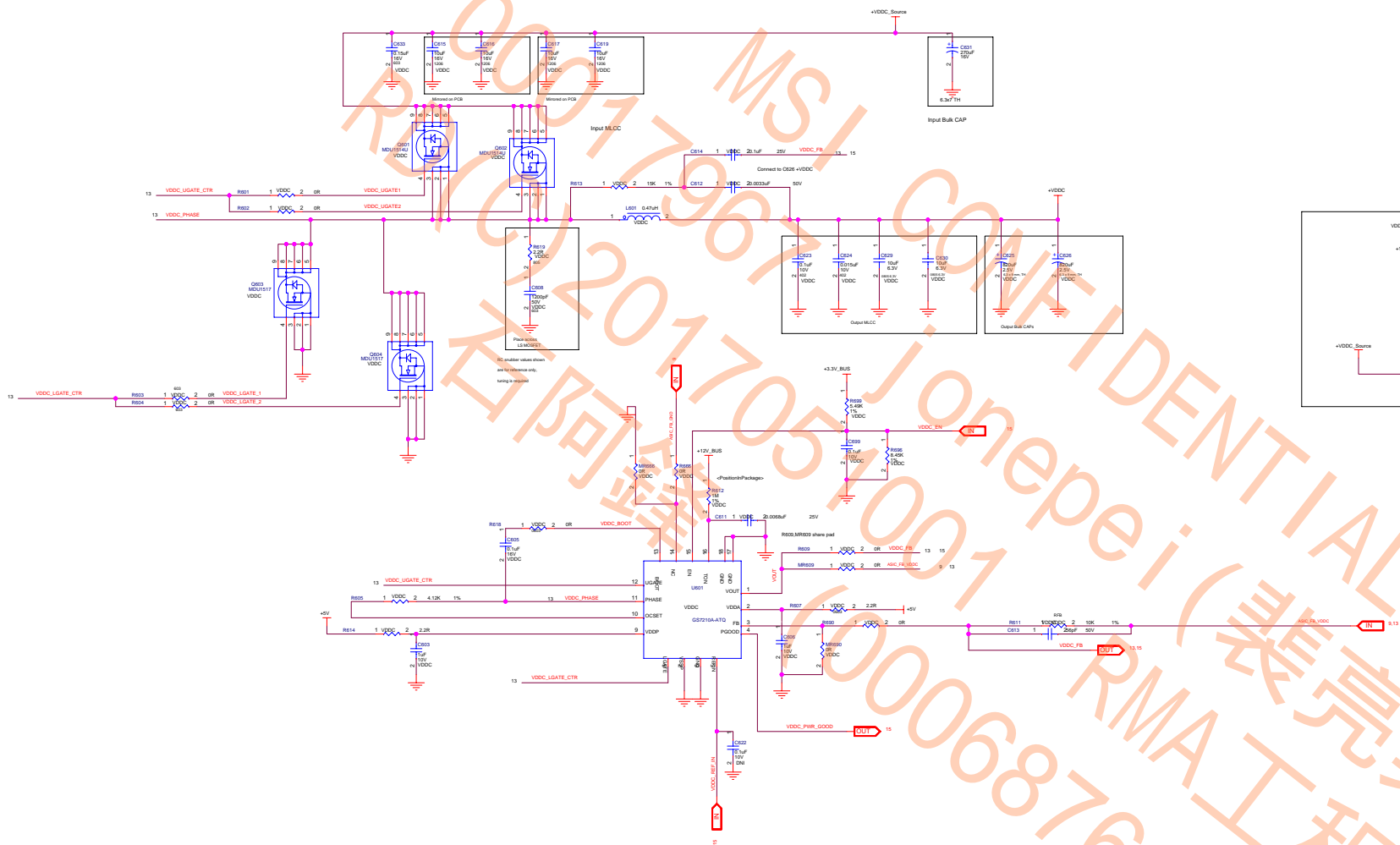
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Regulator for VDDO

Use vVDDC_Sense to share L601 to eliminate PCIe 12V current draw rate over spec (max 1A/us)



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SHEET: VDDO	DATE: Tue Sep 22 06:32:59 2016	REV: 2.0	TITLE: Oland G5 2GB VGA/sDVI-I+HDMI/DP
SHEET NUMBER: 12	OF 20	DOCUMENT NUMBER: 105-C868xx-008	
NOTES: NOTE			



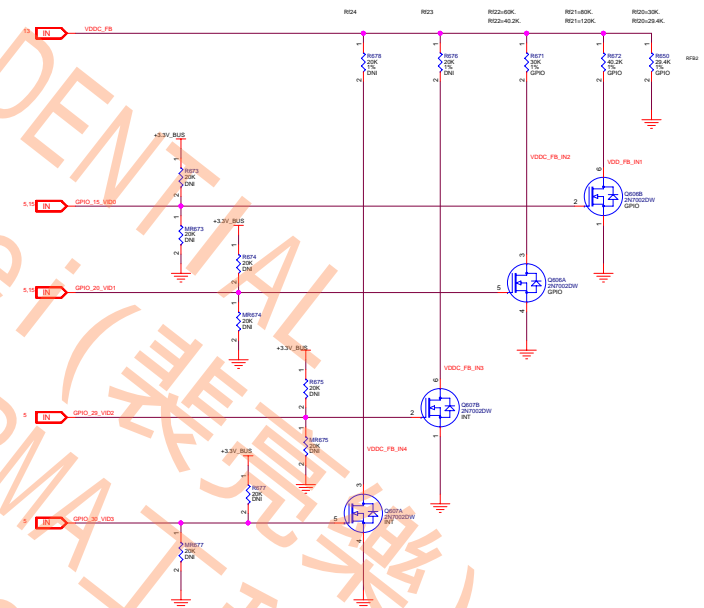
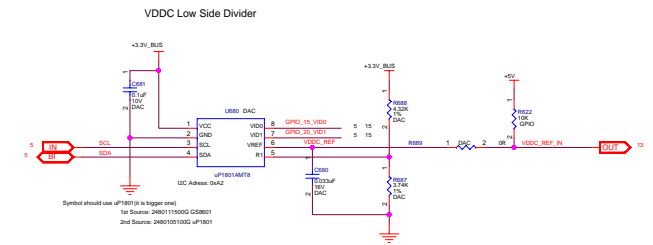
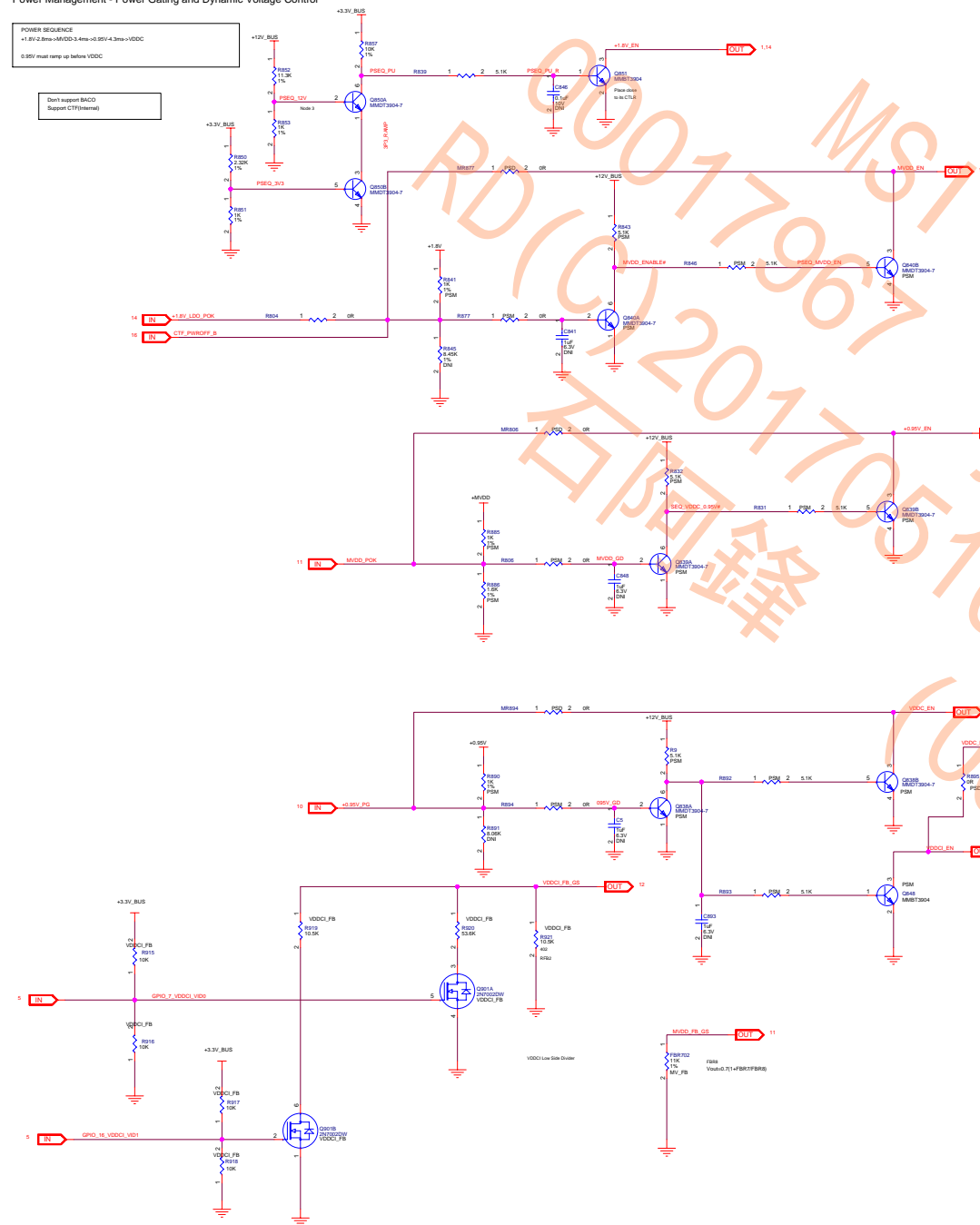
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SHEET: VDDC	
DATE: Mon Sep 21 10:06:41 2015	REV: 2.0
SHEET NUMBER: 13 OF 20	
DOCUMENT NUMBER: 105-C868xx-008	

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TITLE:	Oland G5 2GB VGA/sDVI+HDMI/DP

Power Management - Power Gating and Dynamic Voltage Control

POWER SEQUENCE
+1.8V-2.8ms->MvDD-3.4ms->0.95V-4.3ms->VDDC
0.95V must ramp up before VDDC

Don't support BACO
Support CTF(Internal)



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SHEET: PWR MGMT & SEQ

DATE: Tue Sep 22 02:06:31 2015

REV: 2.0

SHEET NUMBER: 15 15 OF 20 20

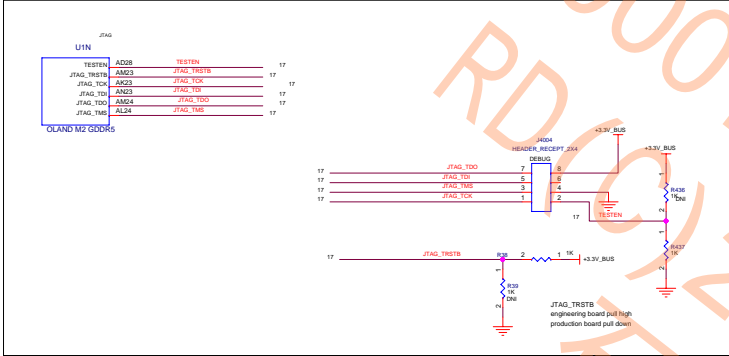
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(19) Debug Circuits



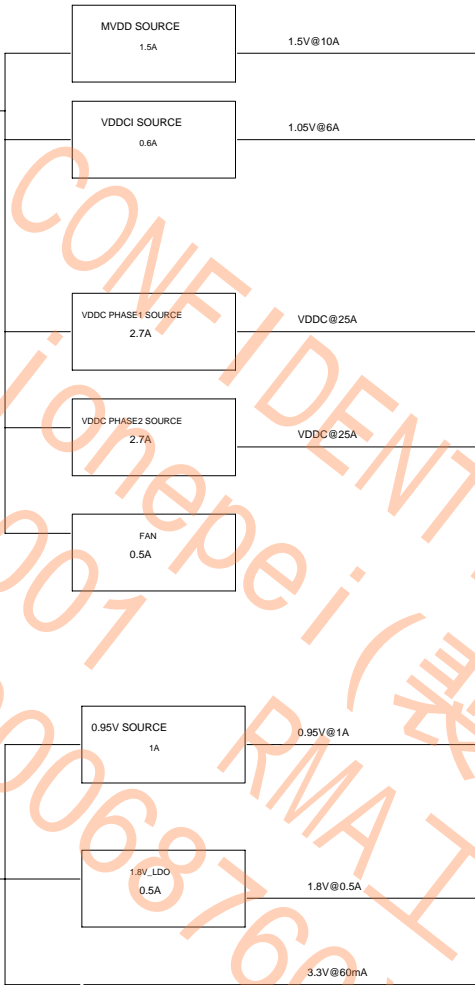
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SHEET:	Debug Circuit		
DATE:	Mon Sep 21 10:06:47 2015	REV:	2.0
SHEET NUMBER:	17	OF	20
DOCUMENT NUMBER:	105-C869xx-008		
TITLE:			Oland G5 2GB VGA/sDV/H+HDMI/DP

DW1	HPD4	DDCAUX4
HDM	HPD1	DDCAUX1
DP	HPD3	DDCAUX3

GPIO15	VDDC_VDD	
GPIO20	VDDC_VD1	
GPIO7	VDDC1_VD	DEFAULT1
GPIO5	VIR_HDT	

12V_BUS
5.5A

3.3V_BUS
3A



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SHEET: GPIO DDC HPD map	
DATE: Tue Sep 22 08:32:59 2015	REV: 2.0
SHEET NUMBER: 18 OF 20	
DOCUMENT NUMBER: 105-C869xx-008	
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TITLE: Oland G5 2GB VGA/sDVI-I+HDMI/DP	

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AMD				TITLE: Oland G5 2GB VGA/sDVI-+HDMI/DP		DOCUMENT NUMBER: 105-C889x-008		DATE: Tue Sep 22 02:20:17 2015		SHEET NUMBER: 20 OF 20		REV: 2.0			
REVISION HISTORY				ENGINEER: Tony Yang		NOTES: NOTE		CONFIDENTIAL AND PROPRIETARY TO ADVANCED MICRO DEVICES INC. This AMD Board schematic and design is the exclusive property of AMD, and is provided only to entities under a non-disclosure agreement with AMD for evaluation purposes. Further distribution or disclosure is strictly prohibited. Use of this schematic and design for any purpose other than evaluation requires a Board Technology License Agreement with AMD. AMD makes no representation or warranty of any kind regarding this schematic and design, including, not limited to, any implied warranty of merchantability or fitness for a particular purpose, and disclaims responsibility for any consequences resulting from use of this information included herein.		AMD - PLATFORM HARDWARE ENG #48, No. 1387, ZHANGDONG ROAD SHANGHAI, CHINA 201203					
SCH Rev		PCB Rev		Date		REVISION DESCRIPTION									
1.00 2.00		000 000		04/19/14 09/22/15		1 Initial release 2 Add VGA, etc									

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